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LINK

Lava I/O News

Inside this issue:

Lava's 8255-PIO

Programmable Peripheral Interface Board

The Lava 8255-PIO (Programmable Peripheral Interface I/O) board is the best way to make use of the I/O capabilities of the 8255 Programmable Peripheral Interface (PPI) chip. This I/O chip is a general purpose programmable device that enables you to manage digital I/O on your PC. It is ideal for use with all Intel and most other processors. The 8255 chip has an 8-bit data bus and provides 24 I/O pins that can be individually programmed in a number of configurations, making this I/O interface product a cost-effective and versatile means of interfacing a microcontroller or other device to a PC. On the Lava 8255-PIO board, the 8255A is implemented in a Xilinx XCS05 FPGA. This is a card worth investigating if you need customizable interfacing using a PC's PCI bus.

The great advantage of the Lava 8255-PIO board is that it makes implementing designs using the 8255 Programmable Peripheral Interface chip easier than ever before, as it now interfaces with the PC using a way familiar with PC users: the PCI bus. It eliminates the need to manually breadboard chips or customize boards, and is ideal as either an interface board for testing products, or as a fully implemented digital I/O method for existing PC systems.

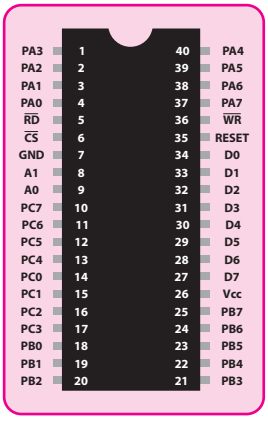
On the device side, the Lava 8255-PIO uses a standard DB-25S connector, for simple and convenient interfacing. This is the same connector used for PC parallel ports; connectors and cables for this side of the board are consequently ready to hand.

The uses for the 8255-PIO are limited by imagination only. One frequent buyer of the Lava 8255-PIO board uses it to interface medical scanners to PCs. He appreciates the higher degree of control that he has over the device by being able to interact so directly with its I/O lines. Another hobbyist uses 8255-PIOs to set up model railroad controls. Yet another uses the 8255's Port A to generate IDE bus control signals for an 8-bit drive controller. Still another uses the 8255 to interface with a PC's printer port to provide parallel port outputs.

With its three 8-bit TTL compatible I/O ports, the 8255-PIO can be used to control up to 24 individual devices. If you want to be able to turn switches on and off from your PC, this is the board for you. Imagine using it to sense door openings, motion, or sound, and to digitally dial a phone number or send e-mail alerts. Does this sound like the basis of a security system?

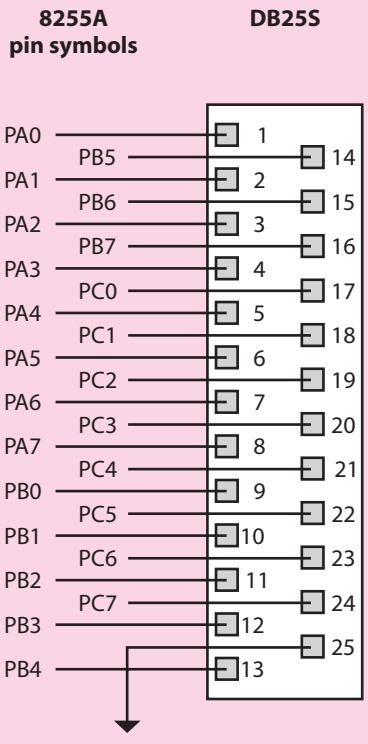
On the industrial side, an 8255-PIO can easily control DC motors, stepper motors, relays and transistors, LCDs, keypads, A/D converters, D/A converters, and so forth. The 8255 is well suited for industrial data acquisition and control. This can be managed locally, or over a network, including the Internet.

The design notes for the Harris Semiconductor version of the 8255 include other interesting methods of employing the 8255 PPI. They illustrate how to interface the 8255 with a printer, a keyboard and display, a keyboard and terminal address, digital-to-analog/analog-to-digital, a basic CRT, a basic floppy disk, or a machine tool. Get out on the web and look at the projects people are undertaking with the 8255 (just try searching on "8255 PPI"). You'll be inspired.



Lava's 8255-PIO emulates the 8255 chip (shown above) in a Xilinx Spartan XCS05 FPGA

Lava 8255-PIO Connector Pinouts



Notes:

PA_{3-0} **Port A, (8255A Pins 0-3)**: Lower nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.

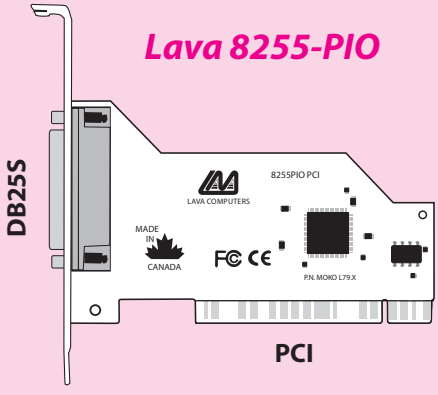
PA_{7-4} **Port A, (8255A Pins 4-7)**: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch.

PB_{0-7} **Port B, (8255A Pins 0-7)**: An 8-bit data output latch/buffer and an 8-bit data input buffer.

PC_{0-3} **Port C, (8255A Pins 0-3)**: Lower nibble of Port C.

PC_{7-4} **Port C, (8255A Pins 4-7)**: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control as specified in manufacturers' data sheets. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

Details on the modes and operation of the 8255A Programmable Peripheral Interface can be found in various manufacturers' specification sheets, some of which are listed in this newsletter's "Sources and useful links" section.



What can the 8255 PPI do?

Although this newsletter does not have the space to give all the details of operation of the 8255 PPI (Programmable Peripheral Interface), describing some of its basic characteristics will give a sense of its versatility. The 8255 PPI has three 8-bit TTL compatible I/O ports, called Port A, Port B, and Port C. In addition, the 8255 has three operating modes that can be applied to these ports (simply called Mode 0, Mode 1, and Mode 2).

Port A (8255 pins PA0-PA7; DB-25 pins 1-8 on the Lava 8255-PIO board) can, depending on the mode selected for the 8255, be programmed with all its bits as input signals, all its bits as output signals, or all its bits as bidirectional lines (both input and output). Port B (8255 pins PB0-PB7; DB-25 pins 9-16 on the Lava 8255-PIO board) can, again depending on the mode selected for the 8255, be programmed with all its bits as input signals, or all its bits as output signals. It cannot operate as a bidirectional port. Port C (8255 pins PC0-PC7; DB-25 pins 17-24 on the Lava 8255-PIO board) can be configured with all its bits as input, or all as output. It can also be split into two 4-bit parts, each of which can be used for input or output. The first 4-bit part of Port C, called CU, consists of the upper four bits of Port C (PC4-PC7); and second 4-bit part of port C, called CL, uses the lower four bits of Port C (PC0-PC3). In some modes Port C can be used to carry handshaking signals for devices, like printers, that would use them. Finally, Port C can allow any individual pin from PC0-PC7 to be individually programmed.

What the different ports are doing at any one time depends on the operating mode (and submode) that the 8255 is using. When in Mode 0, Ports A and B operate either as inputs or outputs and Port C is divided into two 4-bit groups, either of which can be operated as inputs or outputs. Consequently sixteen combinations of port input/output configurations are possible in this mode. Mode 0 is sometimes called "Basic input/output mode."

In Mode 1, Ports A and B operate the same as in Mode 0, but half of Port C is used for handshaking and control for Port A and half of Port C is used for handshaking and control for Port B. Called "Strobed input/output mode," four submode combinations of input and output for Ports A and B exist.

Finally, in Mode 2, Port A operates as a bidirectional port, and five bits of Port C are used for handshaking on Port A. In addition, when Ports A and C are operating in Mode 2, Port B can be configured to operate in Mode 0 or Mode 1. Mode 2, called "Strobed bidirectional bus I/O," along with its possible combination of Port B modes, has therefore got four permutations.

The modes of operation for the 8255 board are selected by writing a special value to the control port. This port is defined as the board's base address + 3. The control codes for configuring the various modes of the Lava 8255-PIO board can be found in 8255 data sheets.

The CPU of the computer holding the Lava 8255-PIO board communicates with the board by sending instructions to its port (not memory) address. In the case of the Lava 8255-PIO, simply use the expansion slot addresses shown in the table below.

This description omits a great deal of secondary detail that would describe the specifics of how precisely to set modes on the 8255, the control signal definitions when the 8255 is using a strobed mode, the specifics of the various 8255 control lines, and other things. However, this newsletter should leave you with a sense of the capabilities of the Lava 8255 board, and perhaps even whet your appetite to investigate this board further.

Programming the 8255 card

Commands to configure and use the Lava 8255 are easily programmed using QBasic, Turbo C, Visual C++, Delphi, Borland C++ or whatever else is familiar and has port I/O functions. Visual Basic can be used if a DLL is written to create the equivalents of QuickBasic's INPUT and OUTPUT functions (or Turbo C's inportb and outportb functions), as these were not implemented in Visual Basic. The URL of a tutorial showing how to write such a DLL is listed in the "Sources and useful links" section of this newsletter.

Other tutorials are also available on the web that show sample code for such programming methods as QBasic. All of these are extremely simple; getting the Lava 8255-PIO board up and running is really very easy!

ADDRESS (HEX/DEC)	DESCRIPTION	ADDRESS (HEX/DEC)	DESCRIPTION
218-21F (536-543)	AVAILABLE	390-39F (906-927)	AVAILABLE
250-277 (592-631)	AVAILABLE	3AA-3AF (938-943)	AVAILABLE
280-2EF (640-751)	AVAILABLE	3B0-3BF (944-959)	AVAILABLE
300-31F (768-799)	AVAILABLE	3F8-3FF	COM 1

Sources and useful links:

- CAST, Inc., *C8255A Programmable Peripheral Interface HDL Core Datasheet,* June 2001 http://www.cast-inc.com/cores/c8255a/c8255a.pdf
- Harris Semiconductor, *82C55A CMOS Programmable Peripheral Interface*, June 1998. File no. 2969.2. This version of the 8255 design notes includes a selection of 8255 application examples in addition to the content of the Intel design notes for the 8255.
- http://www.boondog.com/ — Provides a number of tutorials on projects that can be managed with a PC-based 8255-PIO interface board. A 70-page Applications Manual is also for sale.
- http://www.boondog.com/tutorials/8255/8255.htm — Describes how to create your own 8255 interface board for the ISA bus. But a PCI board from Lava is a better idea.
- http://www.boondog.com/tutorials/dlltutor/dlltutor.htm — Details on how to create a DLL that will make Visual Basic able to read and write to hardware ports, such as those of the 8255.
- http://www.decisioncards.com/io/tutorials/8255_tut.html — A good illustration of using QBasic to program the 8255.
- http://www.geocities.com/SiliconValley/Bay/4803/io8255.html — General 8255 information written by someone using the 8255 to construct model railroad interfaces.
- http://www.phanderson.com/printer/8255disc.html — Outlines how to interface a PC's parallel port with an 8255 PPI. It includes both a wiring diagram and programming code in C.
- http://www.pjrc.com/tech/8051/ide/wesley.html — Describes interfacing an IDE controller to an 8255 PPI.
- Intel, *82C55A CHMOS Programmable Peripheral Interface Design Notes*, October 1995. Order Number 231256-004. Thorough discussion of the modes of operation and methods of configuring the 8255 chip.
- Mohammad Ali Mazidi and Janice Gillespie Mazidi, *The 80x86 IBM PC and Compatible Computers*. Vols. I & II. (Assembly Language, Design, and Interfacing). Englewood Cliffs, NJ: Prentice Hall, 1995. Good discussion of I/O design and the 8255 chip.